In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1-24. (Canceled).

25. (Currently Amended) A whole chip electrostatic discharge ECD method comprising the steps of:

connecting all input/output, I/O pads to each other with double isolation; and

inserting a circuit of the first embodiment of this invention between each adjacent I/O pair on a semiconductor chip, wherein the first embodiment comprises;

a PN diode whose p-side connects to the input/output, I/O pad to be protected and whose N-side is connected to Vcc supply voltage;

a PMOS FET plus NMOS FET 2-device input stage connected between Vcc and Vss;

a resistor plus NMOS FET first mid stage connected between Vcc and Vss (ground);

a resistor to ground second mid-stage; and

a PMOS FET plus NMOS FET output stage connected between Vec and Vss (ground) whose input connects from the mid-stages and whose output drives an unused I/O pad.

26. (Canceled)

27. (Currently Amended) A whole chip electrostatic discharge ECD method comprising the steps of:

connecting all input/output, I/O pads to each other with double isolation, and

inserting a circuit of the second embodiment of this invention between each adjacent I/O pair on a semiconductor chip, wherein the second embodiment comprises:

a PN diode whose p-side connects to the input/output,

I/O pad to be protected and whose N-side is connected to Vcc supply voltage,

a PMOS FET plus NMOS FET 2-device input stage connected between Vcc and Vss,

a resistor plus NMOS FET first mid stage connected between Vcc and Vss (ground),

a second mid-stage containing a second NMOS FET connected between input stage and ground, and

a PMOS FET plus NMOS FET output stage connected between Vcc and Vss (ground) whose input connects from the mid stages and whose output drives an unused I/O pad.

28. (Canceled).